IN THE SPECIFICATION:

Please amend the specification as follows:

Page 9, line 27 through page 3, line 7 (the paragraph straddling page 9 and page 10): please replace this paragraph with the following rewritten paragraph:

The 15 keys, with associated masks, along with the search key and the address generated from stage L0 are the input to this stage. This stage selects the smallest entry that is greater than or equal to the input search key. If multiple entries have the same key, the key with the smallest priority is selected. Again, if no entries are greater than the supplied key, the 4-bit value of the selected entry is the value 15 ~~16~~. The position of the selected element, combined with the address of the row selected by the L0 stage, is the output of this block. Thus, in this embodiment, the 5-bit address from the output of the L0 stage is concatenated with the 4-bit value indicating which of the 16 elements was selected. The resulting 9-bit address is passed to the L2 stage.

Page 10, lines 19 through 27: please replace this paragraph with the following rewritten paragraph:

The 15 keys with associated priorities, along with the search key and the address generated from stage L2 are the input to this stage. This stage selects the smallest entry that is greater than or equal to the input search key. If multiple entries have the same key, the key with the smallest priority is selected. Again, if no entries are greater than the supplied key, the 4-bit value of the selected entry is the value 15 ~~16~~. The position of the selected element, combined with the address of the row selected by the L1 stage, is the output of L2. Thus, in

this embodiment, the 9-bit address from the output of the L1 stages is concatenated with the 4-bit value indicating which of the 16 elements was selected. The resulting 13 bit address is passed to the L2 stage.